What is claimed is:

1. A semiconductor memory device comprising:

a plurality of banks, each having first and second cell mats, each having a plurality of word lines;

a data access controller for selecting a word line from the first cell mat and the second cell mat in response to the row address and a refresh signal to be used in a refresh operation; and

a bank controller for sequentially enabling the first cell mat and the second cell mat in response to a bank address and the refresh signal.

2. The semiconductor memory device as recited in claim 1, wherein the bank controller enables the first cell mat firstly, then, after a predetermined time, enables the second cell mat at the refresh operation.

3. The semiconductor memory device as recited in claim 2, wherein the first cell mat is enabled in response to a first cell mat enable signal.

4. The semiconductor memory device as recited in claim 3, wherein the second cell mat is enabled in response to a second cell mat enable signal.

5. The semiconductor memory device as recited in claim 4,

wherein the bank controller includes:

a first control unit for generating the first cell mat enable signal in response to the bank address;

a refresh period setting unit for generating a refresh period setting signal in response to the refresh signal; and

a second control unit for receiving the first cell mat enable signal and the refresh period setting signal to generate the second cell mat enable signal.

6. The semiconductor memory device as recited in claim 5, wherein the second control unit outputs the first cell mat enable signal as the second cell mat enable signal at a data access operation or outputs the first cell mat enable signal as the second cell mat enable signal after delaying the first enable signal for the predetermined time at the refresh operation.

7. The semiconductor memory device as recited in claim 6, wherein the second control unit includes a delay unit for delaying the first cell mat enable signal.